THAT WHICH IS CLAIMED IS:

1. An improved 2-bit boundary scan test circuit capable of applying boundary scan test vectors to a core logic input, comprising:

a multiplexing means for selectively coupling an output of a boundary scan register to an input of a boundary scan register or to the core logic input; and

a selection mechanism for controlling the multiplexing means to enable the coupling when test vectors are required to be applied to the core logic input.

2. An improved 2-bit boundary scan test circuit as in claim 1 further comprising means to self test the boundary scan circuit.

3. A method for improving a 2-bit boundary scan test circuit to provide the capability of applying boundary scan test vector to a core logic input, comprising:

providing a multiplexing arrangement to enable the selective coupling of the output of a boundary scan test register to the core logic input; and

selectively enabling the multiplexing arrangement for coupling the output of the boundary scan test register when the test vectors are required to be applied to the core logic input.

4. The method of claim 3 further comprising enabling EXTEST and INTEST instructions to operate independently.

5. The method of claim 3 further comprising enabling EXTEST and INTEST instructions to operate simultaneously.

6. An boundary scan test circuit comprising:

first and second multiplexers for receiving a shift/capture control signal;

first and second capture registers coupled to the first and second multiplexers;

first and second update registers coupled to the first and second capture registers;

third and fourth multiplexers coupled to the first and second update registers for receiving a mode control signal;

a buffer section coupled to the third and fourth multiplexers and to a pad; and

a first four-input multiplexer receiving the mode control signal and having at least one input coupled to the first multiplexer and at least one input coupled to the third multiplexer.

7. The boundary scan test circuit of claim 6 further comprising means for enabling EXTEST and INTEST instructions to operate independently.

8. The boundary scan test circuit of claim 6 further comprising means for enabling EXTEST and INTEST instructions to operate simultaneously.

9. The boundary scan test circuit of claim 6 further comprising means for testing a bi-directional pad.

10. The boundary scan test circuit of claim 6 further comprising a second four-input multiplexer having at least one input coupled to an input of the first four-input multiplexer.

11. The boundary scan test circuit of claim 6 further comprising a second four-input multiplexer having at least one input coupled to an output of the first four-input multiplexer.

12. The boundary scan test circuit of claim 6 wherein an output of the fourth multiplexer provides a control signal for the first four-input multiplexer.